WHAT IS CLAIMED IS:

1. A method of routing an electrical trace on a circuit board to reduce noise induced from a reference plane, the method comprising:

routing a first path for an electrical trace on a circuit board such that the first path references a voltage plane;

routing a second path for the electrical trace on the circuit board such that the second path references a ground plane whereby the second path is substantially similar to the first path; and

electrically coupling the first path to the second path at each of the ends of the first and second paths such that noise induced into the electrical trace is reduced.

2. The method of Claim 1, further comprising:

inducing a first noise in the first path with a current traveling in the voltage plane; and

inducing a second noise in the second path with the current returning on the ground plane, whereby the second noise is approximately equal to but opposite of the first noise.

3. The method of Claim 1, further comprising forming a mirror image of the first path with the second path.

4. The method of Claim 1, further comprising forming the voltage plane and the ground plane symmetrically on the circuit board.

5. The method of Claim 4, further comprising disposing the first path and the second path symmetrically on the circuit board.

6. The method of Claim 5, further comprising arranging the first path to the voltage plane such that a mirror image is formed with the second path to the ground plane with respect to a centerline.

7. The method of Claim 1, wherein the electrically coupling the first path to the second path further comprising:

forming an electrically isolated opening in the voltage plane and in the ground plane to allow for a via to connect at one end of the first path to the second path.

8. A circuit board, comprising:

a voltage plane forming a first layer of the circuit board, the voltage plane operable to provide an electrical current;

a ground plane forming a second layer of the circuit board, the ground plane operable to provide a ground for the electrical current;

an electrical trace routed over a portion of the circuit board, the electrical trace including a first path and a second path such that the first path references the ground plane and the second path references the voltage plane whereby the first path is substantially similar to the second path; and

the first path electrically coupled to the second path at each of the ends of the paths such that noise induced into the electrical trace is reduced.

9. The circuit board of Claim 8, wherein the ground plane and the voltage plane are symmetrically oriented with respect to the circuit board.

10. The circuit board of Claim 9, wherein the first path and the second path are symmetrically oriented with respect to the circuit board.

11. The circuit board of Claim 10, wherein the first path and the voltage plane are a mirror image of the second path and the ground plane.

12. The circuit board of Claim 8, wherein the first path electrically coupled to the second path at each of the ends of the paths further comprising:

an electrically isolated opening in the voltage plane operable to connect the first path to the second path.

13. The circuit board of Claim 8, wherein the first path electrically coupled to the second path at each of the ends of the paths further comprising:

an electrically isolated opening in the ground plane operable to connect the first path to the second path.

14. The circuit board of Claim 8, wherein the first path is located at a distance from the voltage plane that is substantially equal to the distance the second path is located from the ground plane.

15. The circuit board of Claim 8, wherein the voltage plane and the ground plane are formed close together on the circuit board.

16. An information handling system comprising:

a processor;

a memory communicatively coupled to the processor; and

a circuit board having an electrical trace, the circuit board operable to reduce noise on the electrical trace induced from a reference plane, the circuit board including:

a voltage plane forming a first layer of the circuit board, the voltage plane operable to provide an electrical current;

a ground plane forming a second layer of the circuit board, the ground plane operable to provide a ground for the electrical current;

an electrical trace routed over a portion of the circuit board, the electrical trace including a first path and a second path such that the first path references the ground plane and the second path references the voltage plane whereby the first path is substantially similar to the second path; and

the first path electrically coupled to the second path at each of the ends of the paths such that noise induced into the electrical trace is reduced.

17. The information handling system of Claim 16, wherein the first path is located at a distance from the ground plane that is substantially equal to the distance the second path is located from the voltage plane.

18. The information handling system of Claim 16, wherein the ground plane and the voltage plane are symmetrically oriented about the circuit board.

19. The information handling system of Claim 18, wherein the first path and the second path are symmetrically oriented about the circuit board.

20. The information handling system of Claim 19, wherein the first path and the ground plane are a mirror image of the second path and the voltage plane.